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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,309	10/03/2003	Tetsuo Suzuki	243579US0X	9488

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EXAMINER	
ARANCIBIA, MAUREEN GRAMAGLIA	

ART UNIT	PAPER NUMBER
1792	

NOTIFICATION DATE	DELIVERY MODE
04/02/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/677,309	SUZUKI ET AL.	
	Examiner	Art Unit	
	Maureen G. Arancibia	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, and 5-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2 February 2008 has been entered.

Claim Objections

2. Claims 8, 9, 11, and 12 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Specifically, Claims 8, 9, 11, and 12 recite claim limitations now recited in independent Claim 1 as amended.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, and 14-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 3,923,567 to Lawrence (from Applicant's IDS) in

view of U.S. Patent 6,100,167 to Falster et al. and U.S. Patent 5,837,662 to Chai et al.

In regards to Claims 1 and 25, Lawrence teaches a method of reclaiming silicon wafers that includes, in the following order, a film removal process (Column 5, Lines 52-65), a heating/removal process (Column 6, Lines 6-33 and Line 49 - Column 7, Line 31), a polishing process (Column 7, Lines 32-38), and a cleaning process (Column 7, Lines 38-40), wherein the heating / removal process is between the film removal process and the polishing process and comprises heating the silicon wafer (Column 6, Lines 6-33) and a chemical process carried out "in air" in that the chemical processing tank would be surrounded by air, that comprises removing a surface part of the silicon wafer by etching the top surface of the silicon wafer (Column 6, Line 49 - Column 7, Line 24).

In regards to Claims 1 and 25, Lawrence does not expressly teach that the heating of the silicon wafer is performed at 150-300°C for 20 minutes - 5 hours. In regards to Claim 15, Lawrence does not expressly teach that the heating step of the heating/removal process is carried out in air. In regards to Claim 16, Lawrence does not expressly teach that the maximum temperature is 300°C.

Falster et al. teaches in a method of reclaiming silicon wafers (Column 1, Lines 11-13) a heating / removal process comprising heating the silicon wafer at 100-300°C for a preferred time of several to several tens of minutes up to about 1.5 hours. (Column 3, Line 61 - Column 4, Line 10) These ranges in temperature and time meet the limitations recited in Claim 1. Falster et al. further teaches that heating process can

be carried out in air (Column 4, Lines 16-18), and that the maximum temperature can be 300°C (Column 4, Line 3).

(The Examiner also observes that Falster et al. (Column 3, Lines 51-60) further teaches that the time is a result-effective variable that affects the diffusion of copper to the surface of the silicon wafer, and is selected in accordance with the heating temperature.)

It would have been obvious to one of ordinary skill in the art to replace the heating step of the heating / removal process taught by Lawrence with the heating step taught by Falster et al. The motivation for making such a modification, as taught by Falster et al. (Column 2, Line 67 - Column 3, Line 50), would have been to diffuse copper to the surface of the silicon wafer without the undesirable copper precipitates that form when the heating is performed at higher temperatures. Moreover, Falster et al. expressly teaches that the heating step taught by Falster et al. is an improvement over prior art gettering methods, since the high diffusivity of copper in silicon makes it possible for copper to escape from the gettering sites and reach the device region of the wafer. (Column 1, Line 64 - Column 2, Line 3)

Further in regards to Claims 1, 23, and 24, the combination of Lawrence and Falster et al. does not expressly teach that the chemical removal step can be performed using alkaline (i.e. basic) hydroxides and/or alkaline carbonates.

Chai et al. teaches that a chemical removal step can be performed using alkaline hydroxides and/or alkaline carbonates, including sodium or potassium hydroxide or sodium or potassium carbonate. (Column 4, Lines 4-7)

It would have been obvious to one of ordinary skill in the art to use one or more of the alkaline hydroxides and/or alkaline carbonates taught by Chai et al. in the chemical removal step taught by the combination of Lawrence and Falster et al. The motivation for making such a modification, as taught by Chai et al. (Column 4, Lines 24-34), would have been that the alkaline bath changes the surface potential of the silicon wafer, causing contaminants to be electrostatically repelled from the surface.

In regards to Claim 2, Lawrence teaches that the heating / removal process can further include a mechanical removal process (Column 7, Lines 25-31).

In regards to Claims 14, 17, and 18, the heating step of the heating/removal process taught by the combination of Lawrence and Falster et al. is carried out so as to provide a *P-type silicon wafer* having the same specific resistance of a virgin (i.e. unused) P-type silicon wafer, as broadly recited in the claims. (Falster et al., Column 1, Line 11 - Column 2, Line 50; Column 3, Line 12 - Column 4, Line 18; Column 5, Lines 14-29) The heating step of the heating/removal process as taught by the *combination* of Lawrence and Falster et al. would inherently not form any oxygen donors, since the process is performed below 300°C and no dopant is introduced into the wafer. This rejection is based on the fact that the method taught by the *combination* of Lawrence and Falster at al. would inherently result in the reclaimed wafer having the recited properties. When a rejection is based on inherency, a rejection under 35 U.S.C. 102 or U.S.C. 103 is appropriate. (See *In re Fitzgerald* 205 USPQ 594 or MPEP 2112).

In regards to Claims 19, 20, and 22, Lawrence teaches that the method can be carried out to reclaim silicon wafers that were previously used as testing wafers to carry

out the monitoring of a semiconductor chip manufacturing process. (*The wafers can be classified as process monitor test wafers…*; Column 1, Lines 30-40; Column 5, Lines 32-35)

In regards to Claim 21, the wafer reclamation method taught by the combination of Lawrence and Falster would inherently produce a silicon wafer without Cu contamination, as broadly recited in the claim (i.e. produce a silicon wafer with a level of contaminants at or below that of a virgin wafer), since the process taught by the combination of Lawrence and Falster et al. is carried out so as to remove contaminants and provide a *P-type silicon wafer* having the same specific resistance of a virgin (i.e. unused) P-type silicon wafer, as discussed above. This rejection is based on the fact that the method taught by the *combination* of Lawrence and Falster at al. would inherently result in the reclaimed wafer having the recited properties. When a rejection is based on inherency, a rejection under 35 U.S.C. 102 or U.S.C. 103 is appropriate. (See *In re Fitzgerald* 205 USPQ 594 or MPEP 2112).

In regards to Claim 26, Lawrence teaches that the chemical process typically etches the top surface of the wafer to a depth of 0.3 to 0.5 mils, or about 7.6 to about 17.8 microns. (Column 7, Lines 11-21)

Lawrence does not expressly teach that the chemical process etches the top surface of the wafer to a depth of only about 1 micron.

However, Lawrence teaches that it is preferable to first determine the depth of the initial diffusion in the semiconductor product to assure that all of the P/N junctions and impurities are removed from the front and back faces of the wafer.

Consequently, since the desirable depth of etching varies based on the depth of diffusion of impurities in the wafer, it would have been obvious to one of ordinary skill in the art, with a reasonable expectation of success, to modify the method taught by the combination of Lawrence, Falster et al., and Chai et al. to perform the chemical process only long enough to etch the top surface of the wafer to a depth of about 1 micron, in the case where it is determined the impurities have only diffused to such a depth.

5. Claims 5-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawrence in view of Falster et al. and Chai et al. as applied to claim 1 above, and further in view of U.S. Patent 5,932,022 to Linn et al.

The teachings of Lawrence, Falster et al., and Chai et al. were discussed above.

In regards to Claims 5 and 6, the combination of Lawrence, Falster et al., and Chai et al. does not expressly teach that an immersion process for chemically processing the silicon wafer should be performed in addition to the heating / removal process between the film removal process and the polishing process, or that the processing liquid can be any of the liquids recited in Claim 6.

Linn et al. teaches an immersion process for chemically processing a bare silicon wafer should be performed prior to a heating step 115 (Figure 1), wherein the processing liquid can be a mixed solution of hydrogen peroxide, ammonia, and water (SC-1 cleaning solution; Step 101; Column 3, Lines 13-20), or a mixed solution of hydrogen peroxide, hydrochloric acid, and water (SC-2 cleaning solution; Step 109; Column 3, Lines 55-65).

It would have been obvious to one of ordinary skill in the art to modify the combination of Lawrence, Falster et al., and Chai et al. to include an immersion process for chemically processing the wafer just before the heating / removal step, with processing liquids taught by Linn et al. The motivation for making such a modification, as taught by Linn et al. (Column 4, Lines 43-49), would have been to perform the heating step on a wafer with a relatively metal-free, hydrophilic surface, such that the finally processed wafer has an increased minority carrier diffusion length.

In regards to Claims 7, 8, 10, and 11, Lawrence teaches that the heating / removal process can include a mechanical removal process (Column 7, Lines 25-31) and a chemical removal process (Column 6, Line 49 - Column 7, Line 21).

In regards to Claims 9, 12, and 13, the combination of Lawrence, Falster et al., and Chai et al. as applied to Claim 1 above teaches that the chemical removal step can be performed using alkaline hydroxides and/or alkaline carbonates, including any of the compounds recited in Claim 13.

Response to Arguments

6. Applicant's arguments filed 4 February 2008 have been fully considered but they are not persuasive.

In regards to Applicant's argument that it would not have been obvious to include one of the alkaline hydroxides and/or alkaline carbonates taught by Chai et al. in the chemical removal step taught by the combination of Lawrence and Falster et al., because the chemical removal step taught by Lawrence and Falster et al. is an etching step, while that taught by Chai et al. is merely a cleaning step, this argument is not

persuasive. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In the instant case, the teachings of Chai et al. would have suggested to one of ordinary skill in the art to include at least one of the alkaline hydroxides and/or alkaline carbonates taught by Chain et al. in the chemical removal process taught by Lawrence and Falster et al., for the reason as taught by Chai et al. of causing contaminants to be electrostatically repelled from the surface of the wafer. One of ordinary skill in the art would recognize that including such a bath aid could be useful even when a portion of the wafer is to be etched away, so as to provide a contaminant-free finished surface.

In regards to Applicant's argument that Falster teaches a boron-based, p-type dopant annealing step, while Lawrence teaches a phosphorus-based, n-type dopant annealing step, and that therefore it would be non-obvious to use the annealing step of Falster in place of the annealing step of Lawrence; and in regards to Applicant's argument that Lawrence adds phosphorus to the prior art silicon wafer, and thus cannot produce a silicon wafer having the same specific resistance as a virgin silicon wafer, specifically an n-type or p-type silicon wafer, these arguments is not persuasive. Examiner does not disagree that boron, in the context of semiconductor processing, is an p-type dopant, while phosphorus, in the context of semiconductor processing, is an

n-type dopant. However, the salient detail in the instant case is that both Lawrence (Column) and Falster (ex. Column 2, Lines 20-24) are concerned with removing contaminants, i.e. undesired impurities, from ***p-type silicon wafers***. While Lawrence teaches a phosphorus-based *gettering step*, the phosphorus is introduced only temporarily to the *p-type* silicon wafer to be reclaimed in order to facilitate the removal of other *undesired contaminants*, and is removed by the end of the process. (Contaminant impurities in silicon are those atoms in the lattice *other than silicon and the intentionally introduced dopant such as B, P, Sb, or As*... In this invention the formation of a shallow diffused layer containing a high concentration of phosphorus attracts contaminant impurities by providing fresh nucleation sites for Cottrell capture and phosphorus for an impurity - impurity interaction. *In addition, the use of a chemical etch to remove the getter phosphorus diffused layer leaves a silicon lattice substantially free of contaminant impurities which could degrade semiconductor product electrical characteristics.* Column 3, Lines 18-52. Phosphorus, in the method of Lawrence, is not being employed as a permanent dopant to the silicon matrix, but rather as a temporary getterer to remove undesired contaminants. Lawrence thus reclaims a *p-type* silicon wafer with the same specific resistance as a virgin *p-type* silicon wafer -- any p-type dopants are left behind, while undesired contaminants are removed. Falster, on the other hand, teaches an analogous method of removing *undesired contaminants* (ex. copper) from a boron-doped *p-type* silicon wafer. Lawrence and Falster are thus both concerned with the same problem of removing *undesired contaminants* from a p-type silicon wafer. Thus, Examiner maintains that it would have been obvious to one of

ordinary skill in the art, informed by Falster et al.'s teaching that a heating step comprising heating the silicon wafer at 100-300°C for a preferred time of several to several tens of minutes up to about 1.5 hours (Column 3, Line 61 - Column 4, Line 10) diffuses copper to the surface of the silicon wafer without the undesirable copper precipitates that form when the heating is performed at higher temperatures (Column 2, Line 67 - Column 3, Line 50), and *informed by Falster et al.'s teaching that such a heating step is preferable over processes including gettering* as taught by Falster et al.'s prior art, since the high diffusivity of copper in silicon makes it possible for copper to escape from the gettering sites and reach the device region of the wafer (Column 1, Line 64 - Column 2, Line 3), would have been motivated with a reasonable expectation of success to modify the method as taught by Lawrence to *replace* the heating step taught by Lawrence with the heating step of Falster et al., for the predictable result of removing contaminants from the p-type wafer. Furthermore, Applicant has not provided any evidence of unexpected results that would tend to indicate that the claimed method would be non-obvious in view of the teachings of prior art.

In regards to Applicant's argument that the processes of Falster and Lawrence are contradictory to one another because Lawrence requires a gettering temperature that is substantially higher than the annealing temperature of Falster, and that Lawrence would be rendered inoperable by the proposed combination, this argument is not persuasive. That Lawrence teaches a *different* way for removing impurities from a p-type wafer, even that Lawrence teaches what Lawrence believes to be the *best* way ("to

maximize purifying effectiveness;" Column 4, Lines 21-22) does not mean that Lawrence teaches *away* from another way of removing impurities.

In regards to Applicant's argument that Falster does not teach a process whereby a silicon wafer is reclaimed, this argument is not persuasive. Falster teaches a process of removing contaminants from a p-type silicon wafer to produce a p-type silicon wafer without contaminants (ex. Column 2, Lines 20-24); i.e. to reclaim a p-type silicon wafer. Moreover, the primary reference of Lawrence teaches the claimed features wherein the wafer to be reclaimed is a used test wafer, as discussed in the rejection above.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maureen G. Arancibia whose telephone number is (571)272-1219. The examiner can normally be reached on core hours of 10-5, Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571) 272-1435. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Maureen G. Arancibia/
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